seL4 Working Group – CHERI Alliance

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- Objectives
  - Consolidate existing efforts trying to port seL4 to CHERI
  - Coordinate open-source development efforts around CHERI-seL4
  - Have a single CHERI-seL4 (kernel) to reduce confusions with upstreaming and the seL4 community
  - Sync updates, events, demos etc around CHERI-seL4

- Activities
  - Around 4 CHERI Alliance members interested in or working on CHERI-seL4
  - WIP open-source CHERI-seL4 (kernel), with RFC and pull requests submitted upstream
  - Regular monthly meetings

- Get involved
  - Mailing list: wg-sel4@cheri-alliance.org
    - Subscribe: https://lists.cheri-alliance.org/mailman3/
  - Email: hesham.almatary@cheri-alliance.org

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Purecap seL4 kernel, user libraries, and sel4test passing all tests

Firmware

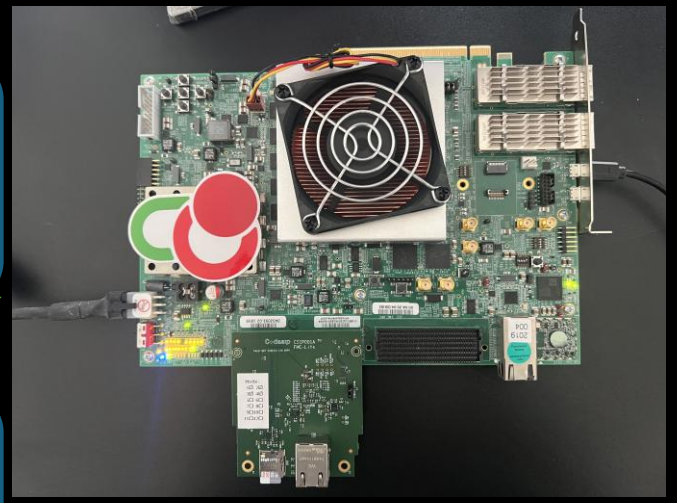
- elfloader: Could optionally be built in purecap for some targets
- OpenSBI: Not purecap yet, but hybrid just to preserve tags and capabilities

Kernel

- PR and RFC submitted to support CHERI-seL4 in the kernel
- CHERI-RISC-V (RV32 and RV64) – 4 new platforms
  - Cambridge's CHERI ISAv9 (e.g., on Toooba-BESSPIN FPGA)
  - CHERI-RISC-V standard specification v0.9.4 (e.g., on Codasip's x730 processor)
- Arm Morello: 4 new platforms submitted – QEMU, FVP, bhyve, and Morello SoC board
- Purecap and hybrid kernel modes
- Enables building and running complete all-purecap seL4 user-space

Userspace

- Able to run complete purecap projects (sel4test and sel4bench)
- All C/C++ seL4 user libraries that sel4test and sel4bench are using are ported to purecap
- sel4test passes all tests in purecap



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