RISC-V: Driving the Future of Open Compute

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RISC-V is an Open Standard Instruction Set Architecture (ISA)

Software uses the ISA to tell the hardware what to do.

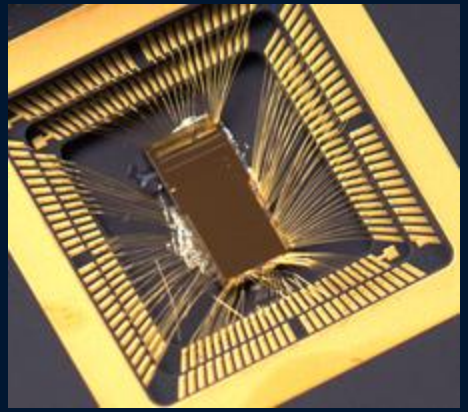
The RISC-V ISA and extensions ratified by RISC-V International are royalty free and open base building blocks for anyone to build their own solutions.

RISC-V International is the global non-profit home of the RISC-V ISA, related specifications, and stakeholder community

Global standards are a catalyst for innovation

Standards have been critical to technology innovation, adoption, and growth for decades

Standards create access to opportunities and spur growth for a wide range of stakeholders



RISC-V is a standards-defined Instruction Set Architecture developed by a global community

RISC-V®

A Global Organization

- Membership
  - ⅓ Asia
  - ⅓ Americas
  - ⅓ Europe
- Contribution from all geographies to Special Interest Groups and Technical Working Groups
- Enabling worldwide RISC-V Innovation

RISC-V is now an ISO/IEC JTC1 PAS Submitter!

Ballot passed in September 2025

- RISC-V International (as a group of members) operates in line with the ISO/IEC JTC1 directives
- Policies and guidelines, our spec development process, our tech committees and voting procedures are fully aligned to JTC1
- RISC-V International is an entity eligible to submit specifications to become ISO/IEC JTC1 published standards
- We will now work to make the RISC-V ISA manuals become ISO/IEC JTC1 standards

RISC-V turned 15 last year!

https://riscv.org/blog/risc-v-15-years/

Invest locally

Engage globally

RISC-V®

The technical foundation for lasting success

Countries

- Tech sovereignty
- Accelerate local innovation and talent
- Incubate technology ecosystem from research to industry
- Access worldwide market

Multinationals

- Control strategic roadmap
- New opportunities for innovation and influence
- Growth business models
- Avoid vendor lock-in

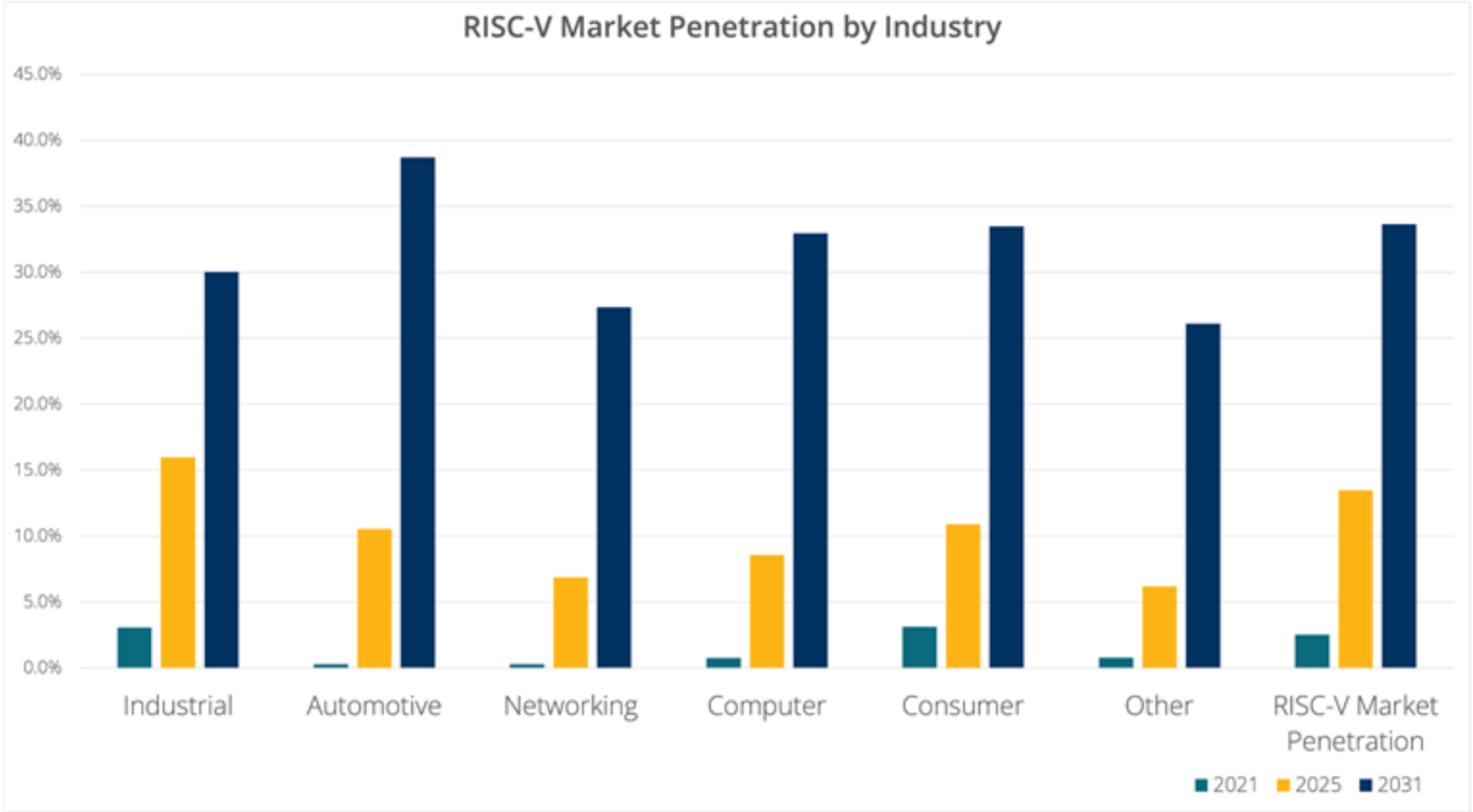
Researchers

- Collaborative ISA thought leadership
- Enables innovative research
- Access global RISC-V research network
- Tech transfer addressing real world applications

Startups

- Supercharge hardware and software co-design
- Accelerate strategic roadmap in greenfield applications
- Collaboration partners

From 2.5% to 33.7% in 10 years!



the SHDgroup

Priority Industry Verticals & Horizontals

Automotive

Data Center

Embedded / IoT

Consumer

HPC

Industrial

Space / Aerospace

Verticals

AI

Security

Horizontals


RISC-V
RVA23 PROFILE

Profiles, Platforms and software ecosystem

Core ISA

ISA Extensions
Floating point,
Bit ops, Vector

non-ISA Extensions
Interrupt controller,
IOMMU

Software Extensions
Boot/Runtime Services
ABI Specification

Custom Extensions
Vendor specific

RVA
Application
Processor

RVB
Embedded
Processor

RVM
Microcontroller

Server

Mobile

Automotive

Embedded System

Edge AIoT/AI

Big Data, Database, LLM
Red Hat Enterprise Linux · Ubuntu · SUSE

Android Apps
Android

Android Auto
Safety Linux

yocto PROJECT
Container runtime

Zephyr · freeRTOS

Extensions
Enable Diversity

Profiles
(mandatory ISA extensions)
Certainty for software

Platforms
(Profile + nonISA + software)
Certainty for OS & firmware

RISC-V

Security

- Security whitepaper: TEEs Using RISC-V Supervisor domains
  - Download from https://riscv.org/security/

- New Security Extensions in Progress
  - SPMP, RISC-V Worlds, IOPMP, Supervisor Domains, CHERI, Lightweight Memory Tagging, Additional Crypto
- CHERI profiles are in progress

CHERI on RISC-V is already delivering new solutuions!

Thank you

RISC-V®