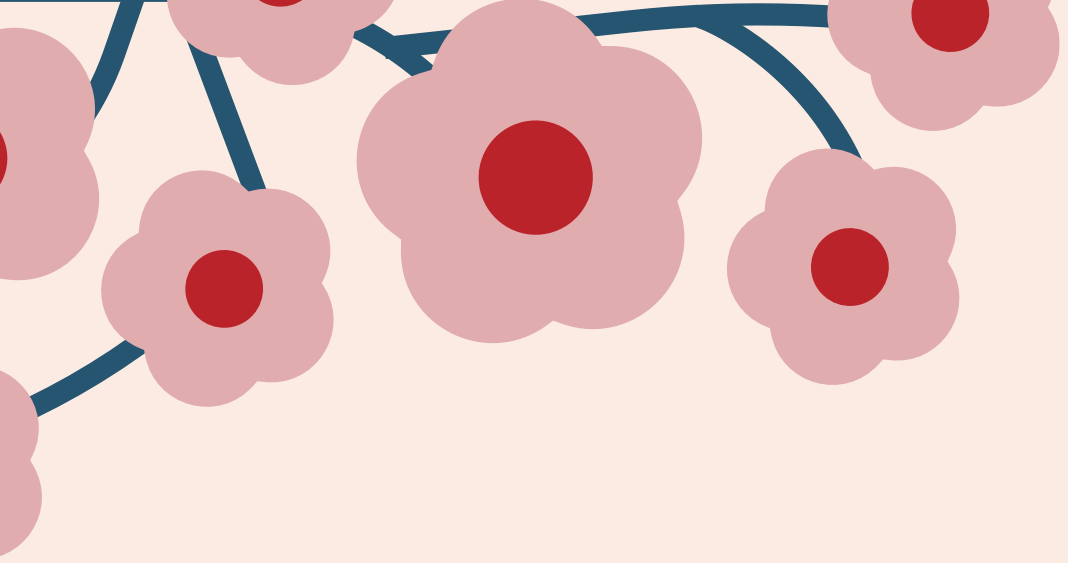
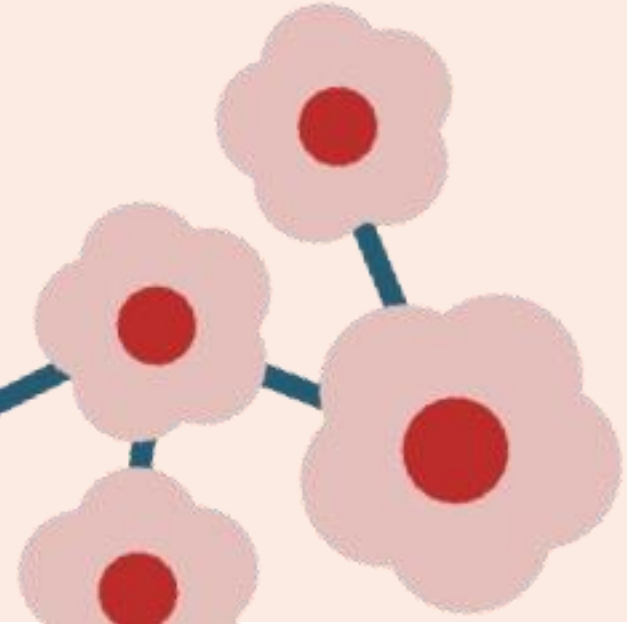
06 April 2026



CHERI

Standardisation Status

Where the specification is now



Author
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Agenda

- RISC-V Ratification Flow
- Where is the CHERI Specification?
- What's the ratification timetable?

Ratification Flow

06 April 2026

CHERI

RISC-V Ratification Flow

- The RISC-V ratification flow goes through several stages
  - See https://riscv.org/specifications/development/
  - **Inception**
    - **The spark that gets things going**
  - **Plan**
    - **Get a plan approved**
  - **Develop**
    - **Create and refine the specification**
  - **Freeze**
    - **Pass architecture review**
  - **Public Review & Ratification Ready**
    - **Literally reviewed by the public, for ~40 days**
  - **Ratified**
    - **Approved by the Board Of Directors**

Where is the CHERI specification?

Freeze checklist

- Trying to reach the freeze milestone
  - This is the key development milestone
  - From this point there can only be changes if serious bugs are found
  - All instruction encodings and mnemonics are complete and cannot change
    - Therefore the toolchain and simulators can be upstreamed
- We have to achieve all the points on the checklist
- The main hurdle is the **Architecture Review**

Architecture Review

- Specification v0.9.7 has been submitted for architecture review
- Previous iterations of the specification have been modified due to feedback from the Architecture Review
  - Simplifying exception reporting
  - Remove exceptions from branches/jumps
  - Rename all mnemonics and CSRs
- We are still waiting for
  - Confirmation of the strategy for declaring multiple capability encoding formats
  - Finalised instruction encodings
  - Finalised CSR addresses

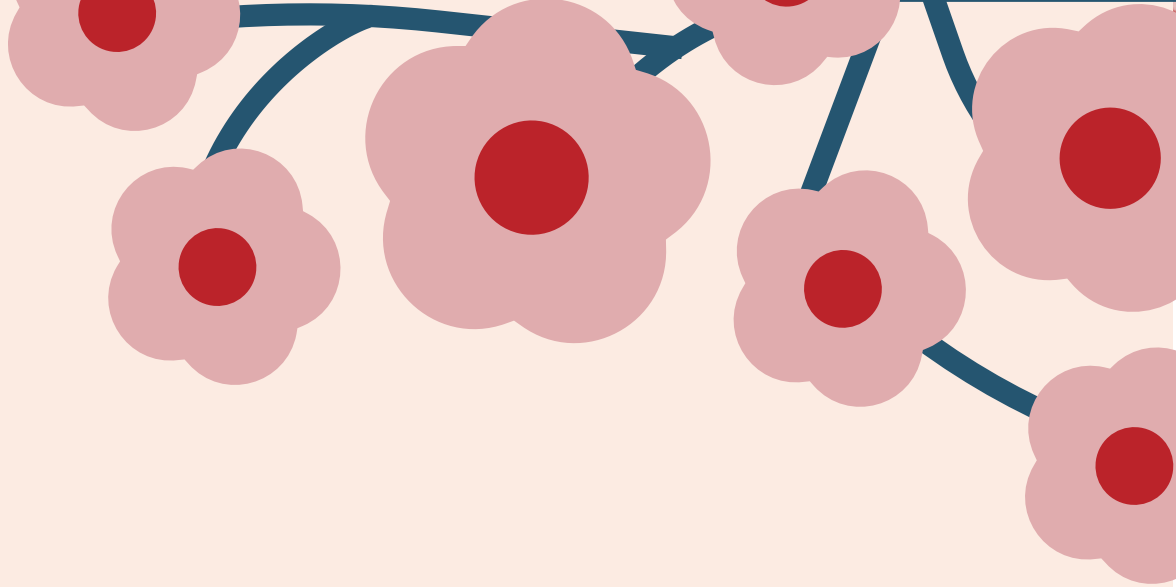
What else do we need for freeze?

- Document complete - yes
- Opcode support – all are specified – none in the custom space
- Simulators – we have SAIL and Qemu
  - They will need updating for all capability formats which are to be frozen
- ABI – draft document – maybe more work needed here?
- Compiler Support – LLVM is available
- Tests – these can be released once the encodings have been frozen, as they need updating
  - Again, these need to include all capability formats
- PoC – Updating at least one core to the approved spec

What's the timetable?

Ratification Timetable – out of date

- Ratification is intended for Q2-2026, but Q3 seems more likely
- We should complete AR in April, then
  - Update LLVM, SAIL, QEmu and tests for the final mnemonics and encodings
  - Go to public review by early June, completing in July
- Ratification ready in August 2026, and then ratified at the next board meeting



CHERI

THANK YOU

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Web www.cheri-alliance.org

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