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CHERI is being standardised,  
so why do we still need to do  
research?

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## ○ **CHERI for RISC-V Standardisation**

### **Criteria for standardisation:**

- ◆ Compelling use-cases
- ◆ Implementations
  - ◆ In hardware
  - ◆ with software support
- ◆ Specification in Sail
- ◆ Simulation support
- ◆ Test suite

See Tariq Kurd's talk on:  
**CHERI RISC-V Standardisation Status**



# ○ Why are we standardising CHERI for RISC-V?

- Many concepts central to CHERI are well understood:
  - Compressed capability format
  - Capabilities for spatial memory safety
  - Capabilities for temporal memory safety (e.g. use-after-reallocation)
  - Capabilities for compartmentalisation
- For all of the above, we understand:
  - ISA-level additions required
  - Compiler, linker and debugger support needed
  - How to build applications, run-time systems and operating systems



## ○ So, aren't we done? Why do research?

- There are parallels with other fundamental computer architecture concepts
- Industry & academia continue to:
  - Refine the use of page tables
  - Explore memory isolation and its weaknesses (e.g. Intel SGX)
  - Refine branch prediction, data pre-fetch, caching, etc.
  - Explore alternative models of computation



## ○ Examples of ongoing investigation

- ◆ New uses for capabilities, e.g. from Ericsson
  - ◆ Conditional capabilities
  - ◆ Blinded capabilities for data-oblivious computation
  - ◆ Coloured capabilities
- ◆ Faster temporal memory safety
- ◆ New compartmentalisation models
  - ◆ E.g. building on library compartmentalisation
- ◆ Security evaluation tools
  - ◆ Are compartment boundaries in the right place?
- ◆ Single address space operating systems using CHERI for isolation



## ○ Conclusions

- ◆ Base CHERI architecture mechanisms are ready for standardisation
- ◆ Many established use-cases built on these mechanisms, but many more to be invented
- ◆ Many hardware/software co-optimisations are possible



# CHERI

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# THANK YOU

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